FDD NewsLetter

September 1991

Vol. 1 No. 4

It's About Time...or What Ever Happened to the FDD NewsLetter?

Allow me to apologize yet again for another delay. Due to circumstances beyond my control, this newsletter is obviously late. It will be short in news due to its lateness. First, I owe an explanation to all of you, especially those who have sent in a contribution. I still promise to produce at least 12 issues - a year's worth.

I got into an minor accident in September and my car was in the shop for a nearly a month. I was carpooling for that period of time. This arrangement prevented me from using the photocopy machine at work to do my newsletter publishing. I normally use the photocopy machine in the late evenings wnen no one is around. You will notice that this month's newsletter contains the FDC 1770 fact sheet. This was a monumental photocopying effort for me, as you can well see. I hope to be out with the October 1991 issue some time between October 31 & November 3. The November 1991 issue should be out some time around November 14 - 17. I hope to be back on schedule (was I ever??) for December 1991. I also hope to have a color print-out then. Can anyone send me an interesting SCREEN$ to use for the December issue. If you do, send it to me on either tape or a CF2 diskette. They will be returned, of course! (Big hint, December...holiday theme!) The second reason that I'm a bit late is that I received a request for some CP/M programs configured for our TMX Portugal FDD system & I got carried away. The person sent me 1 CF2 diskette with an accompanying letter stating, "If you have CP/M programs that you think that I might need feel free to load this disk up". In addition, an automatic line numbering program was requested. Well, let me tell you, I went hog wild! I somewhat laughed to myself thinking that all I was sent was 1 CF2 diskette and asked to fill it up! WordStar 4, CP/M Edition's printer overlays take up a whole 148k, which leaves no room to spare on a diskette! I guessed that since most of you out there have used only T.O.S. - the Timex Extended Disk BASIC, you were still using programs that were memory-limited and not disk-limited. I sent this person the best commercial software that was written for CP/M - 10 diskettes worth! Now, this person's '2068 is no longer running "toy" business programs. It took me over a week to get this all together. I hope that it's appreciated! This also set my schedule back, because I had to key in some documentation with an explanation on how to use the programs I sent. I have a copy now so that any requests in the future for a "CP/M Starter's Kit" will be as easy as 1-2-3. Sorry, no Lotus spreadsheets for CP/M exist!

Lastly, I've been short of funds, typical for a Timex/Sinclair user. I had to shell out $500 of my own to get my car repaired because I've got a $500 deductible. You'll notice that this mailing is extra postage for me. Oh well, so much for my sob story.

Correspondence Dept.

I've gotten newsletter exchanges from the following:

CATS - Capitol Area T/S
ISTUG - Indiana S/T Users Group
LIST - Long Island S/T
Sinc-Link - Toronto T/S Users Club
SWYM - SeaTUG (Seattle, Wa.)
The Hacker - T/S U G of Las Vegas
The Plotter - CCATS (Clackamas County Applied Training Society)

I've even gotten this newsletter mentioned in Bill Ferrebee's column in Computer Monthly magazine. I know that there are a few more newsletters out there being published, such as Nite-Time News from CATUG & the newsletter from SMUG. Is QZX still publishing? I'm a ham myself. Come on, let's get those newsletters coming this way! Another 3 issues & if there is no exchange (or $10 donation), off you go from my exchange mailing list.

First, let me correct some mis-information that appeared in the Sinc-Link's separate preface letter to out-of-town members. It states that the listing on "Random Access and Sequential Data File" by George Gilder...is for use with systems that have the CP/M mode. This is not true. This program listing is for any TMX Portugal FDD system user for use under TOS - the Timex Operating System - an extended disk BASIC that adds disk commands to the T/S 2068 repertoire.

I've managed to track down Kevin Bulgrien in Longview, Texas. "So what?", you say. Well, Kevin has a utility program that he wrote that will allow one to read a TOS disk under CP/M. He says that your file must be at the top directory for this to work. So what, no bells & whistles. I've been looking for a program like that. By the time you're reading this, I'll have exchanged diskettes with him & I'll let you know what I think of it. I was browsing through BBS listings in a computer magazine and saw his name. I left a message on the BBS he was running at the time. He confirmed that he was the Kevin Bulgrien that I saw mentioned in Ron Havlen's FDD Express newsletter. Ron mentioned the TOS - CP/M utility that Kevin wrote. Ron also wrote that he lost track of Kevin after Kevin moved. Kevin now uses IBM micros, but still has an affinity for the T/S 2068 & the FDD system. Welcome back, Kevin!

The September/October 1991 issue of SWYM has an article of particular interest to TOS & CP/M users by Mike Finn. It's called "TOS Revealed by CP/M!". In it, Mike shows how to examine the 1k bootstrap program our system uses when it "boots" up. Great work Mike! Sorry, I've been so busy & broke that I couldn't make the trip to you in Philadelphia this Columbus Day Week-end. I'll try to reschedule this get-together some time soon.

James Brezina writes that maybe Vern Tidwell has the older 3 piece system without CP/M. Well, that thought never crossed my mind. However, Joan Kealy writes, "Yes, Vernon (Tidwell) had CP/M at one time because he wanted to give it to me in a clone case he fashioned for me but I mailed it back. So you are a FRI - SAT night swinger!". No, Joan, I'm an Orthodox Jew, & that's my Sabbath. No computers & the like on my Sabbath. I'm busy learning religious teachings on that day. I never use the computer on the Sabbath. I've really only got 1 day (Sunday) to do any work on the weekend. That's why I'd been hesitant about publishing this newsletter in the first place - I'm short on time as well. More of your letters next issue.

Jack Dohaney is looking for anyone who has attempted to make use of a Centronics interface (such as an AERCo) to work with programs under CP/M instead of the serial port Channel A.

Chuck Kereluck of Seattle is now publishing SWYM & would like any information concerning the use of the serial ports for printers & modems. He has the older 3-piece FDD system & no CP/M. I think Nazir Pashtoon might be able to install CP/M in your FDD. Also, there is a utility program that comes on the DEMO disk with every FDD system that allows you to route your LLIST, LPRINT, & COPY out through Ch A. More next issue!

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New telephone #: 1(718)853-7521

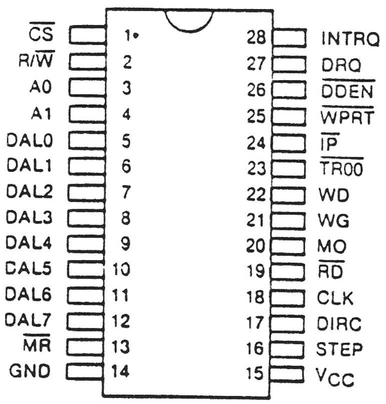
WESTERN DIGITAL
C O R P O R A T I O N

PRELIMINARY

WD1770/1772 5¼" Floppy Disk Controller/Formatter

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- 5¼" SINGLE AND DOUBLE DENSITY
- MOTOR CONTROL
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8 BIT BIDIRECTIONAL DATA BUS
- TWO VERSIONS AVAILABLE
  WD1770 = STANDARD 179X STEP RATES
  WD1772 = FASTER STEP RATES



PIN DESIGNATION

DESCRIPTION

The WD1770 is a MOS/LSI device which performs the functions of a 5¼" Floppy Disk Controller/Formatter. This is similar to its predecessor, the WD179X, but also contains a digital data separator and write precompensation circuitry. The drive side of the interface needs no additional logic except for buffers/receivers. Designed for 5¼" single or double density operation, the device contains a programmable Motor On signal.

The WD1770 is implemented in NMOS silicon gate technology and is available in a 28 pin dual-in-line.

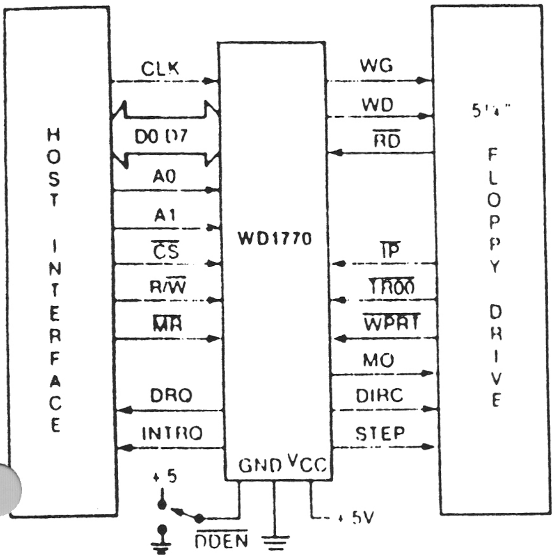
The WD1770 is a low cost version of the FD179X Floppy Disk Controller/Formatter. It is compatible with the 179X, but has a built-in digital data separator and write precompensation circuits. A single read line (RD, Pin 19) is the only input required to recover serial FM or MFM data from the disk-drive. The device has been specifically designed for control of 5¼" floppy disk drives with data rates of 125 KBits/Sec (single density) and 250 KBits/Sec (double density). In addition, write precompensation of 125 Nsec from nominal can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to enable the spindle motor automatically prior to operating a selected drive.

Two versions of the WD1770 are available. The standard version is compatible with the 179X stepping rates, while the WD1772 offers stepping rates of 2, 3, 5 and 6 msec.

The processor interface consists of an 8-bit bidirectional bus for transfer of status, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three "LS" loads.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enable Host communication with the device.
2	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	A logic high on this input controls the placement of data on the $\overline{\text{D0-D7}}$ lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	ADDRESS 0,1	A0, A1	These two inputs select a register to Read/Write data: **$\overline{\text{CS}}$ A1 A0 R/$\overline{\text{W}}$ = 1 R/$\overline{\text{W}}$ = 0** 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DATA ACCESS LINES 0 THROUGH 7	DAL0-DAL7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{\text{CS}}$ and R/$\overline{\text{W}}$. Each line will drive one TTL load.
13	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
14	GROUND	GND	Ground.
15	POWER SUPPLY	V_{CC}	+ 5V ± 5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's R/$\overline{\text{W}}$ head. The WD1770 and WD1772 offer different step rates.
17	DIRECTION	DIRC	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLOCK	CLK	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ± 1%.
19	$\overline{\text{READ DATA}}$	$\overline{\text{RD}}$	This active low input is the raw data line containing both clock and data pulses from the drive.
20	MOTOR ON	MO	Active high output used to enable the spindle motor prior to read, write or stepping operations.
21	WRITE GATE	WG	This output is made valid prior to writing on the diskette.
22	WRITE DATA	WD	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This active low input informs the WD1770 that the drive's R/$\overline{\text{W}}$ heads are positioned over Track zero (internal pull-up).
24	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette (internal pull-up).
25	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).
26	$\overline{\text{DOUBLE}}$ DENSITY ENABLE	$\overline{\text{DDEN}}$	This input pin selects either single (FM) or double (MFM) density. When $\overline{\text{DDEN}}$ = 0, double density is selected (internal pull-up).

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	DATA REQUEST	DRQ	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTERRUPT REQUEST	INTRQ	This active high output is set at the completion of any command or reset a read of the Status Register.



WD1770 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RD) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

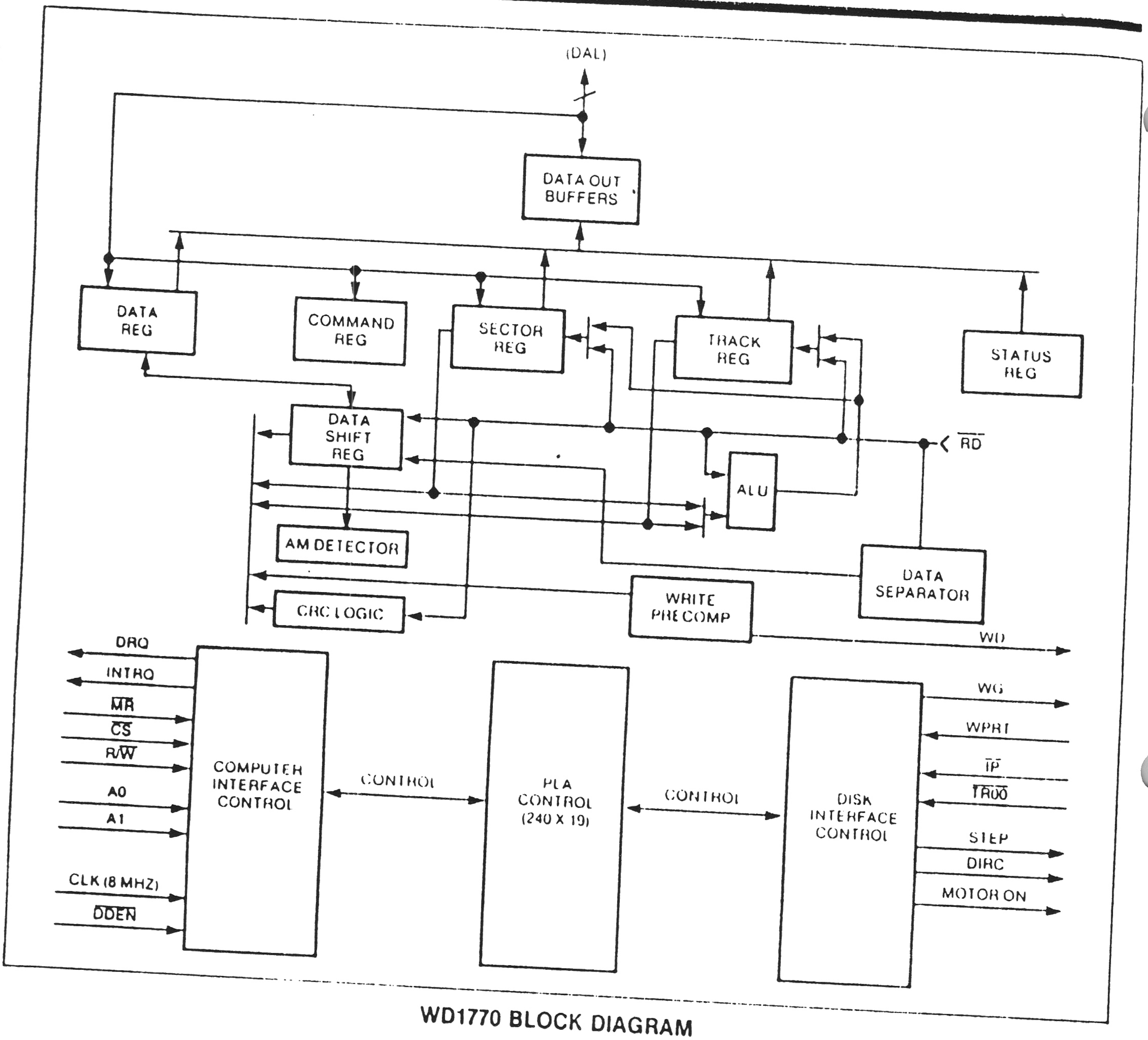
Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:
$G(x) = x^{16} + x^{12} + x^{5} + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.



WD1770 BLOCK DIAGRAM

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The FD1770 has two different modes of operation according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}}$ = 0, double density (MFM) is enabled. When $\overline{\text{DDEN}}$ = 1, single density is enabled.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Data Separator — A digital data separator consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1770. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{\text{CS}}$) and $\text{R}/\overline{\text{W}} = 1$ are active or act as input receivers when $\overline{\text{CS}}$ and $\text{R}/\overline{\text{W}} = 0$ are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{\text{CS}}$ is made low. The address bits A1 and A0, combined with the signal $\text{R}/\overline{\text{W}}$ during a Read operation or Write operation are interpreted as selecting the following registers:

A1	A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1770 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD1770 has two modes of operation according to the state $\overline{\text{DDEN}}$ (Pin 26). When $\overline{\text{DDEN}}$ = 1, single density is selected. In either case, the CLK input (Pin 18) is at 8 MHZ.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per tract as far as the WD1770 is concerned can be from 1 to 255 sectors. The number of tracks as far as the WD1770 is concerned is from 0 to 255 tracks.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For Write operations, the WD1770 provides Write Gate (Pin 21) to enable a Write condition, and Write Data (Pin 22) which consists of a series of active high pulses. These pulses contain both Clock and Data Information in FM and MFM. Write Data provides the unique missing clock patterns for recording Address Marks.

The Precomp Enable bit in Write commands allow automatic Write precompensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nanoseconds according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

Next Bit to be sent
Current Bit sending
Previous Bits sent

Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximun.

COMMAND DESCRIPTION

The WD1770 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-Up Sequence
h = 1, Disable Spin-Up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1, 0)

r_1,	r_0	WD1770	WD1772
0	0	6 ms	2 ms
0	1	12 ms	3 ms
1	0	20 ms	5 ms
1	1	30 ms	6 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

a_0 = Data Address Mark (Bit 0)

a_0 = 0, Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

E = 30ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 30ms Delay

P = Write Precompensation (Bit 1)

P = 0, Enable Write Precomp
P = 1, Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = 1, Don't Care
I_1 = 1, Don't Care
I_2 = 1, Interrupt on Index Pulse
I_3 = 1, Immediate Interrupt
I_3-I_0 = 0, Terminate without Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0,r_1), which determines the stepping motor rate.

A 4µs (MFM) or 8 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24µs before the first stepping pulse is generated.

After the last directional step an additional 30 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 30 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation.

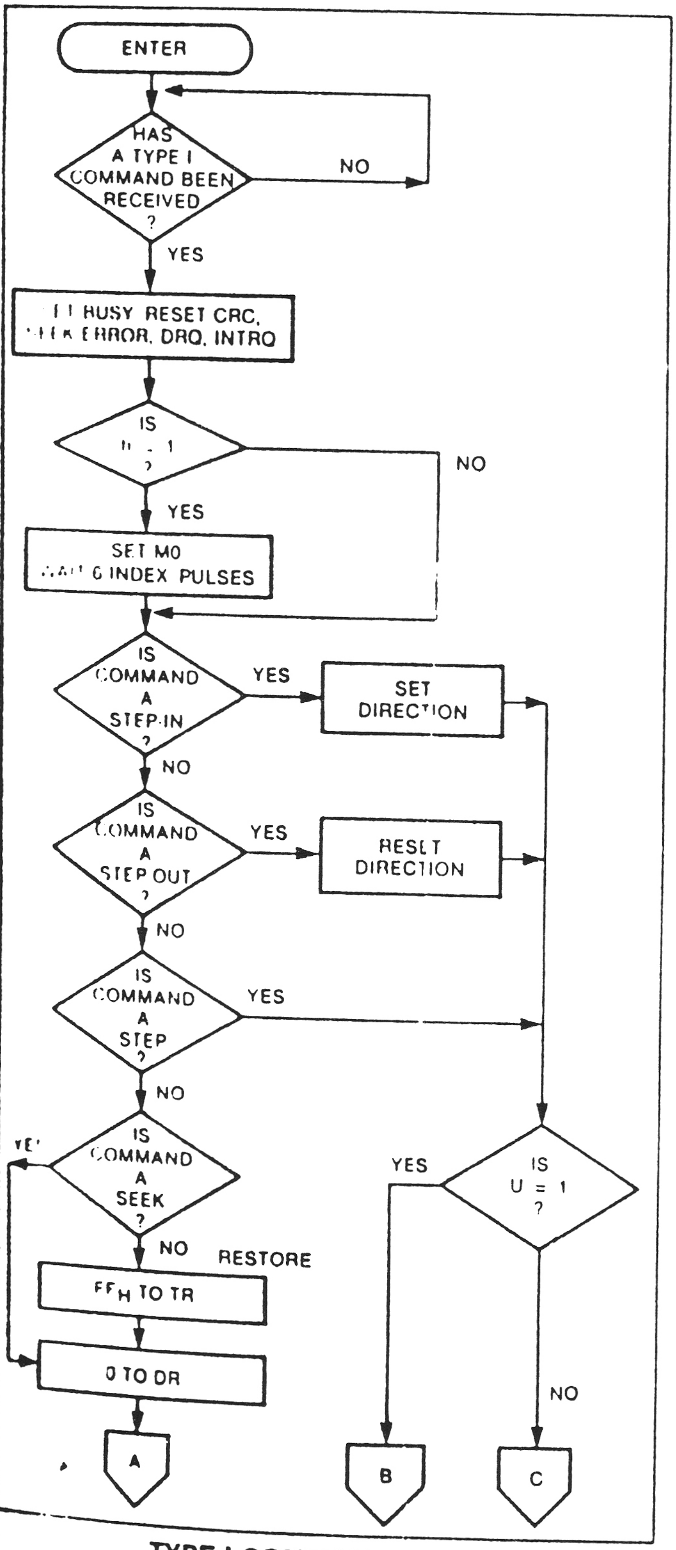
The WD1770 must find an ID field with correct track number and correct CRC within 5 revolutions of the media, otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed

All commands, except the Force Interrupt command may be programmed via the h Flag to delay for spindle motor start up time. If the h Flag is set and the Motor On line (Pin 20) is low when a command is received, the WD1770 will force Motor On to a logic 1 and wait 6 revolutions before executing the command. At 300 RPM, this guarantees a one second spindle start up time. If after finishing the command the device remains idle for 10 revolutions, the Motor

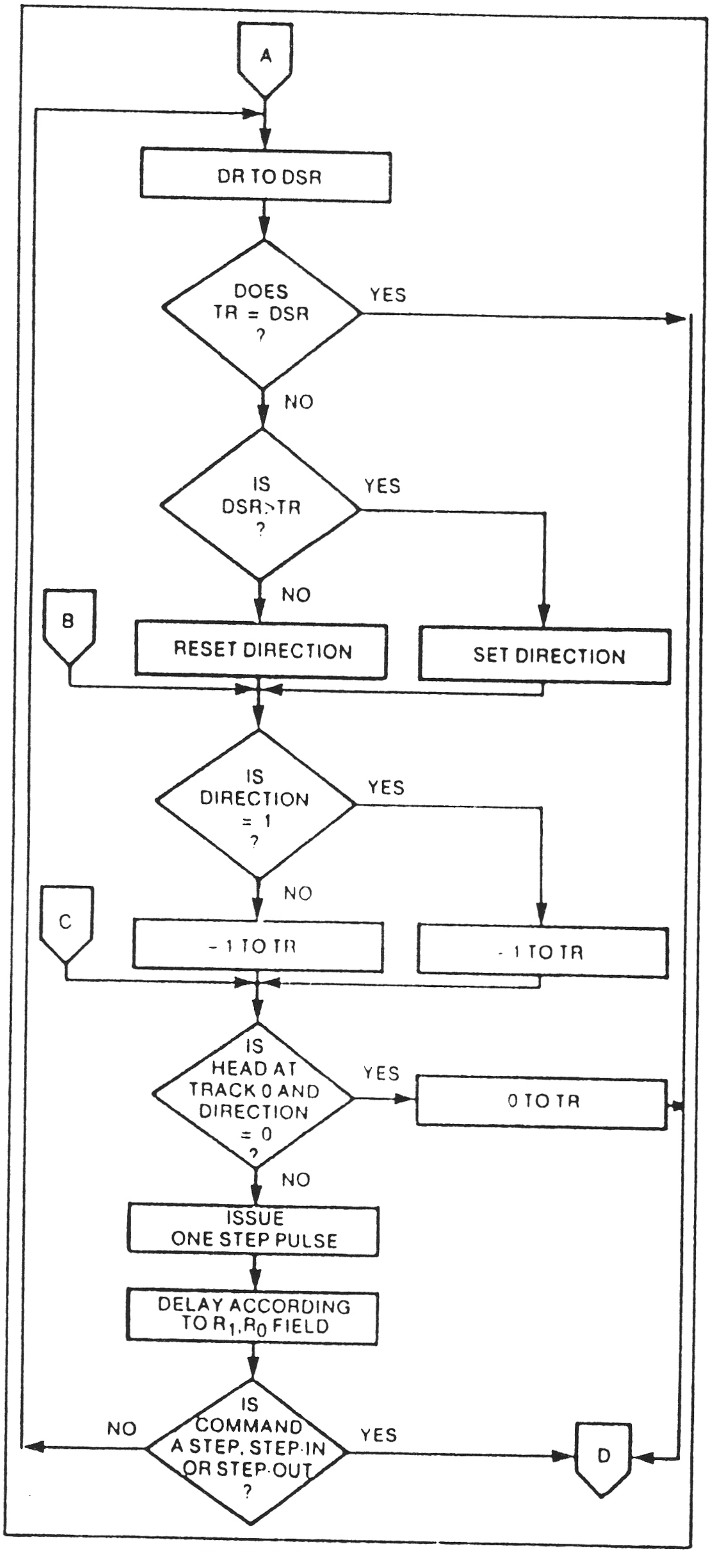
On line will go back to a logic 0. If a command is issued while Motor On is high, the command will execute immediately, defeating the 6 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1770 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 ($\overline{\text{TR00}}$) input is sampled. If $\overline{\text{TR00}}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not active low, stepping pulses (Pin 16) at a rate specified by the r_1,r_0 field are issued until the $\overline{\text{TR00}}$ input is activated.



TYPE I COMMAND FLOW

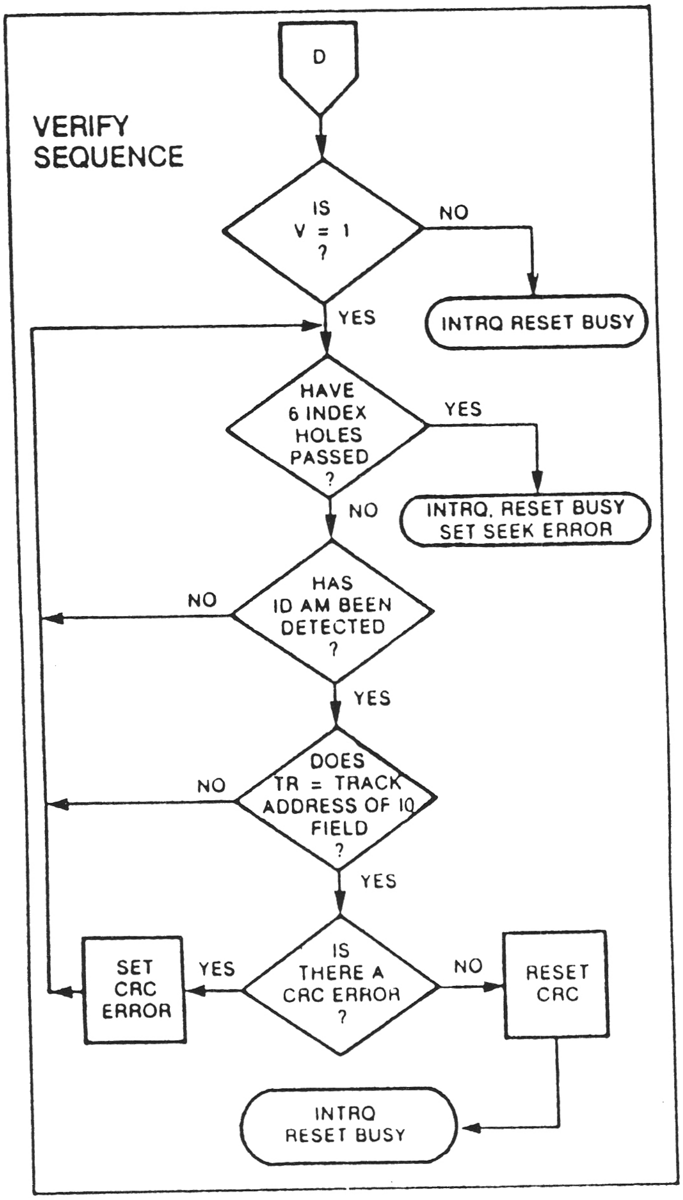


TYPE I COMMAND FLOW

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TR00}}$ input does not go active low after 255 stepping pulses, the WD1770 terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD1770 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.



TYPE I COMMAND FLOW

STEP

Upon receipt of this command, the WD1770 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD1770 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

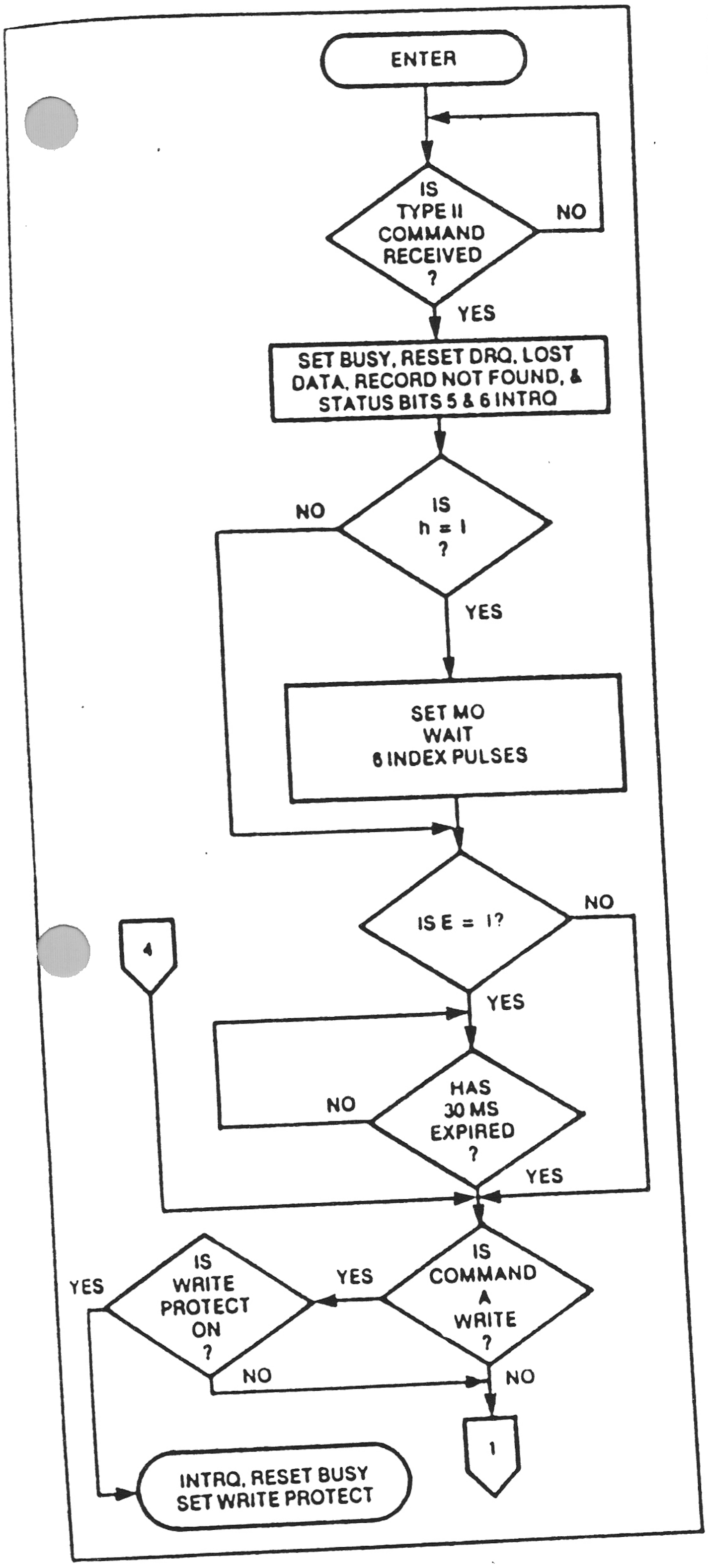
STEP-OUT

Upon receipt of this command, the WD1770 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After delay determined by the r_1,r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1 the command will execute after a 30 msec delay.

When an ID field is located on the disk, the WD1770 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The WD1770 must find an ID field with a Track number, Sector number, and CRC within four revolutions of the disk, other-


ENTER
IS TYPE II COMMAND RECEIVED ?
NO
YES
SET BUSY, RESET DRQ, LOST DATA, RECORD NOT FOUND, & STATUS BITS 5 & 6 INTRQ
IS h = 1 ?
NO
YES
SET MO WAIT 6 INDEX PULSES
IS E = 1?
NO
YES
4
HAS 30 MS EXPIRED ?
NO
YES
IS COMMAND A WRITE ?
YES
NO
IS WRITE PROTECT ON ?
YES
NO
1
INTRQ, RESET BUSY SET WRITE PROTECT

TYPE II COMMAND

wise, the Record not found status bit is set (Status Bit 4) and the command is terminated with an interrupt (INTRQ).

ch of the Type II Commands contains an (m) flag hich determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The WD1770 will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD1770 is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The WD1770 will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

READ SECTOR

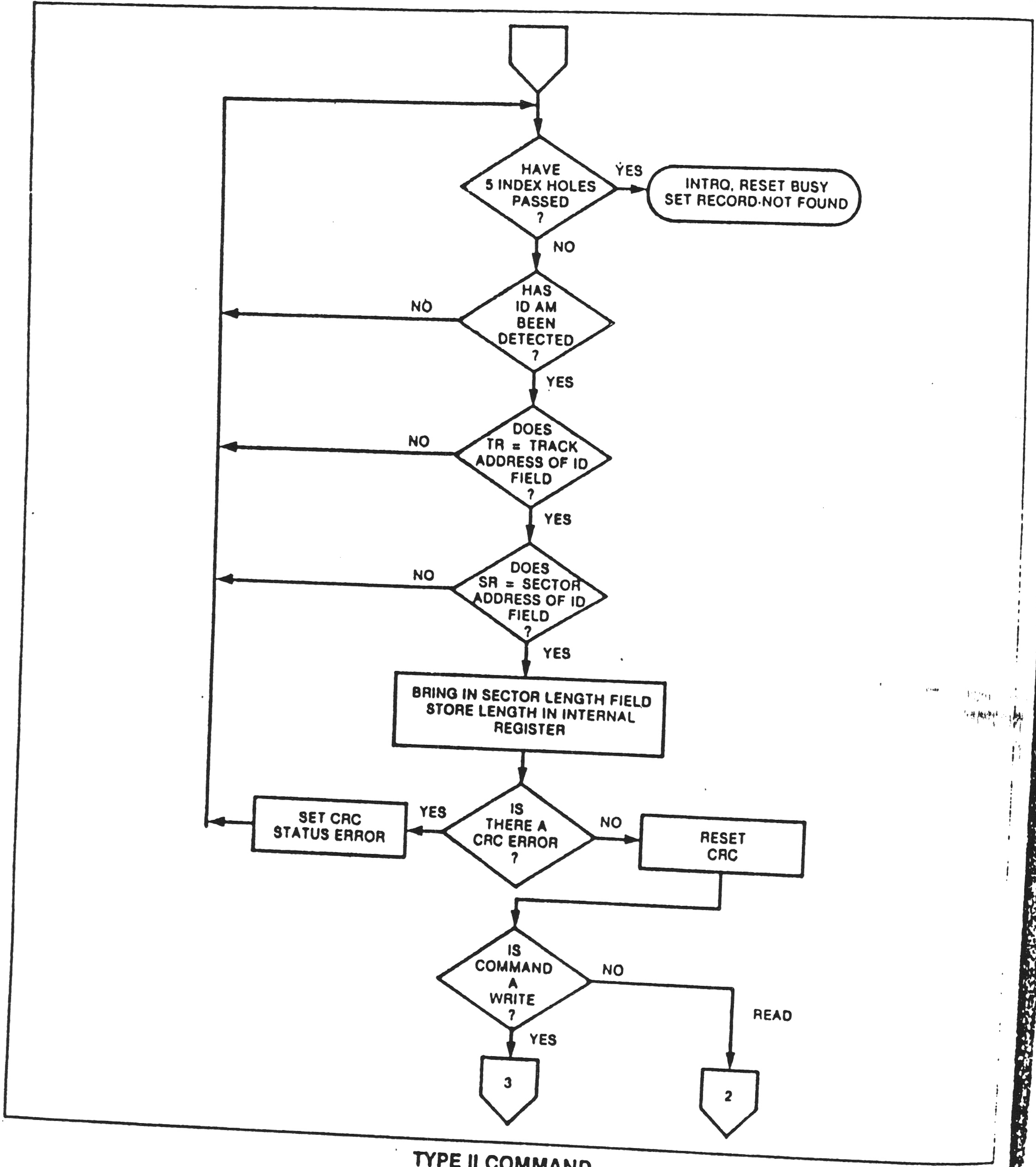
Upon receipt of the Read Sector command, the Busy status bit is set, and when a ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The WD1770 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated

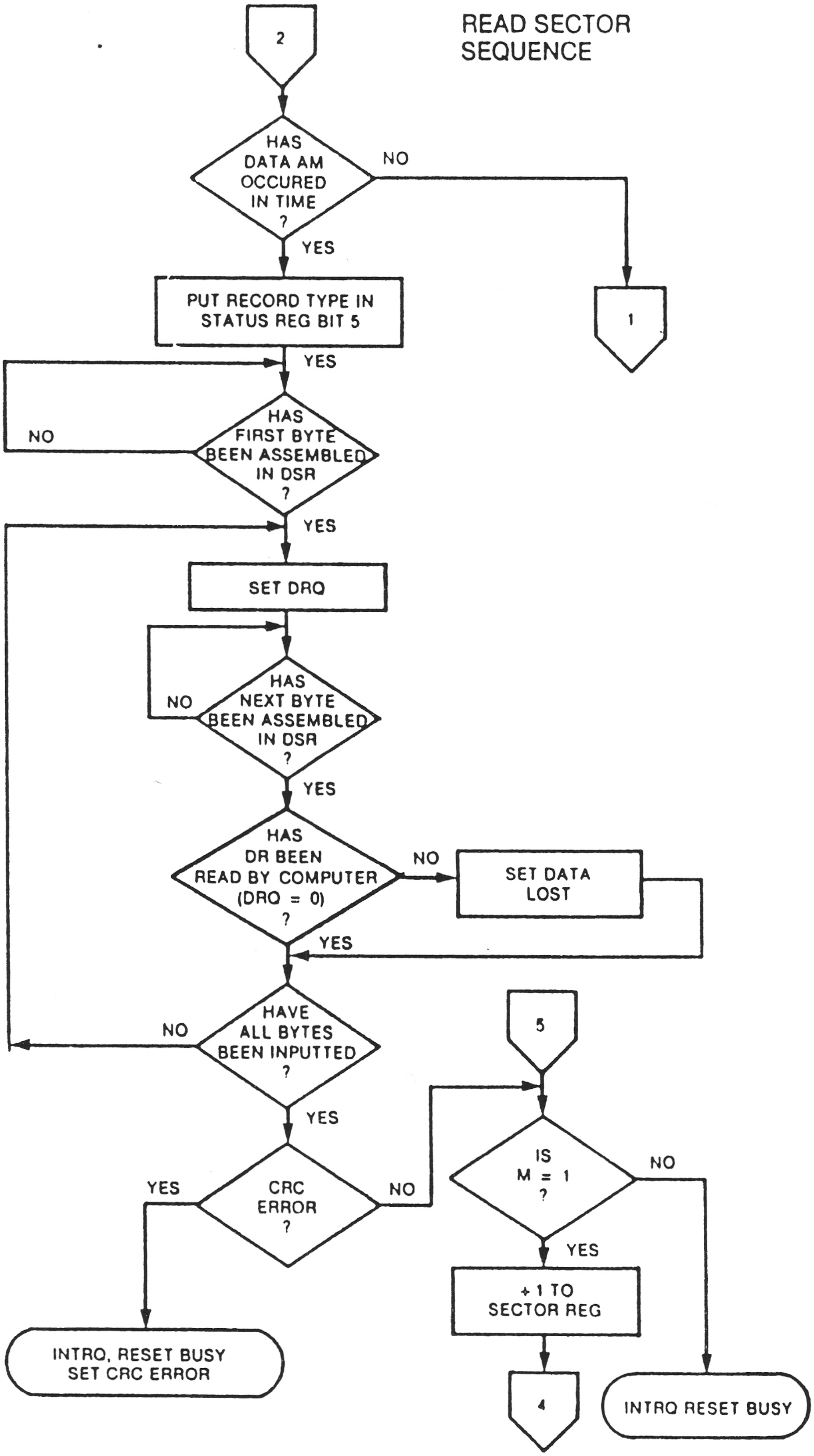

HAVE 5 INDEX HOLES PASSED ?
YES
INTRQ, RESET BUSY SET RECORD NOT FOUND
NO
HAS ID AM BEEN DETECTED ?
NO
YES
DOES TR = TRACK ADDRESS OF ID FIELD ?
NO
YES
DOES SR = SECTOR ADDRESS OF ID FIELD ?
NO
YES
BRING IN SECTOR LENGTH FIELD STORE LENGTH IN INTERNAL REGISTER
IS THERE A CRC ERROR ?
YES
SET CRC STATUS ERROR
NO
RESET CRC
IS COMMAND A WRITE ?
NO
READ
YES
3
2

TYPE II COMMAND

and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time, the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

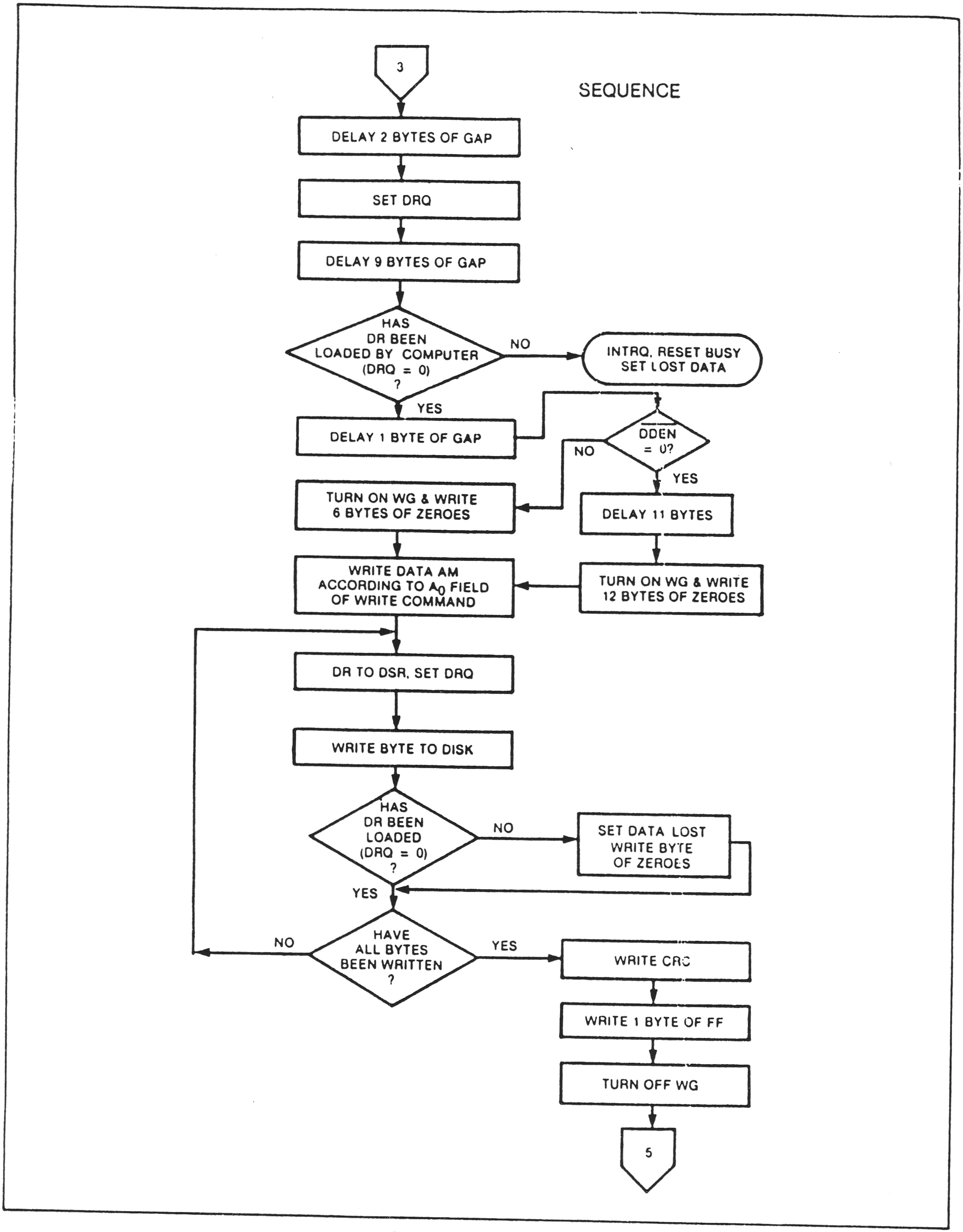
The WD1770 then writes the data field and generate DRQ's to the computer. If the DRQ is not serviced time for continuous writing the Lost Data Status B



READ SECTOR SEQUENCE

2
HAS DATA AM OCCURED IN TIME ?
NO
YES
1
PUT RECORD TYPE IN STATUS REG BIT 5
YES
HAS FIRST BYTE BEEN ASSEMBLED IN DSR ?
NO
YES
SET DRQ
HAS NEXT BYTE BEEN ASSEMBLED IN DSR ?
NO
YES
HAS DR BEEN READ BY COMPUTER (DRQ = 0) ?
NO
SET DATA LOST
YES
HAVE ALL BYTES BEEN INPUTTED ?
NO
YES
5
CRC ERROR ?
YES
NO
IS M = 1 ?
NO
YES
+1 TO SECTOR REG
INTRQ, RESET BUSY SET CRC ERROR
4
INTRQ RESET BUSY

TYPE II COMMAND


3
SEQUENCE
DELAY 2 BYTES OF GAP
SET DRQ
DELAY 9 BYTES OF GAP
HAS DR BEEN LOADED BY COMPUTER (DRQ = 0) ?
NO
INTRQ, RESET BUSY SET LOST DATA
YES
DELAY 1 BYTE OF GAP
DDEN = 0?
NO
YES
TURN ON WG & WRITE 6 BYTES OF ZEROES
DELAY 11 BYTES
WRITE DATA AM ACCORDING TO A0 FIELD OF WRITE COMMAND
TURN ON WG & WRITE 12 BYTES OF ZEROES
DR TO DSR, SET DRQ
WRITE BYTE TO DISK
HAS DR BEEN LOADED (DRQ = 0) ?
NO
SET DATA LOST WRITE BYTE OF ZEROES
YES
HAVE ALL BYTES BEEN WRITTEN ?
NO
YES
WRITE CRC
WRITE 1 BYTE OF FF
TURN OFF WG
5

TYPE II COMMAND

is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ will set 24μsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address

Upon receipt of the Read Address command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD1770 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the READ track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

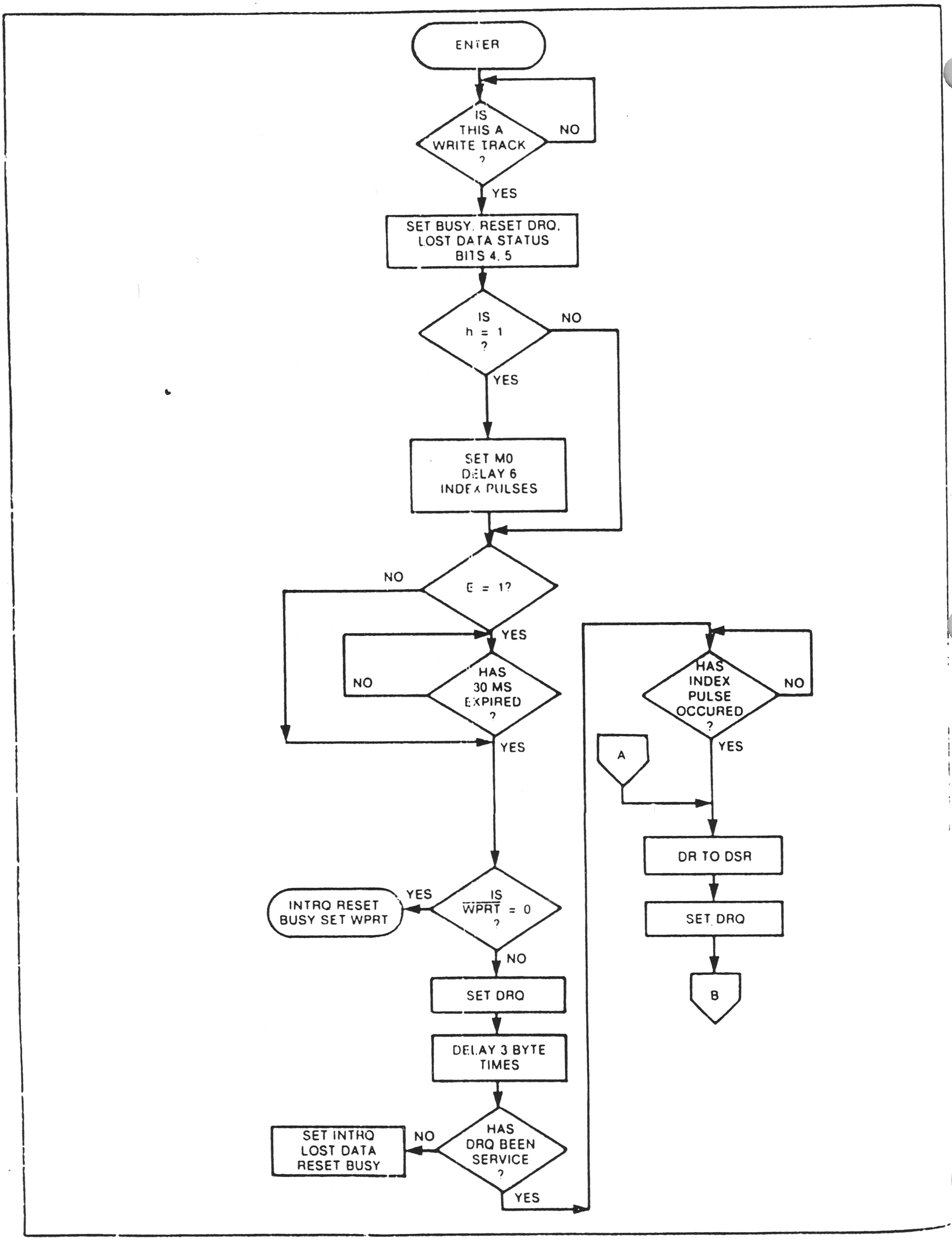
Upon receipt of the Write Track command, the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded within 3 byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the WD1770 detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

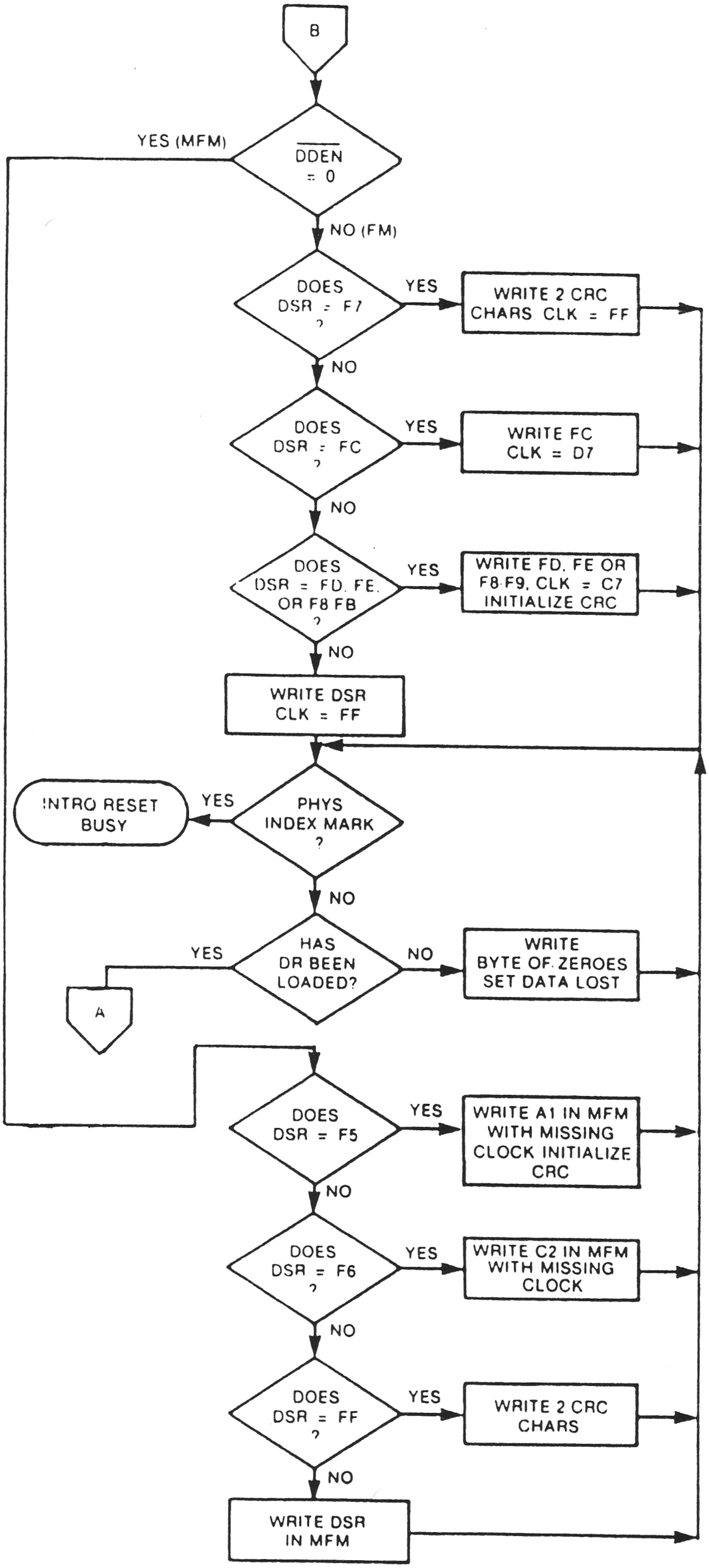
DATA PATTERN IN DR (HEX)	IN FM ($\overline{\text{DDEN}}$ = 1)	IN MFM ($\overline{\text{DDEN}}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.

**Missing clock transition between bits 3 and 4.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Don't Care
I_1 = Don't Care
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 micro sec (double density) or 32 micro sec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

RECOMMENDED — 128 BYTES/SECTOR

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

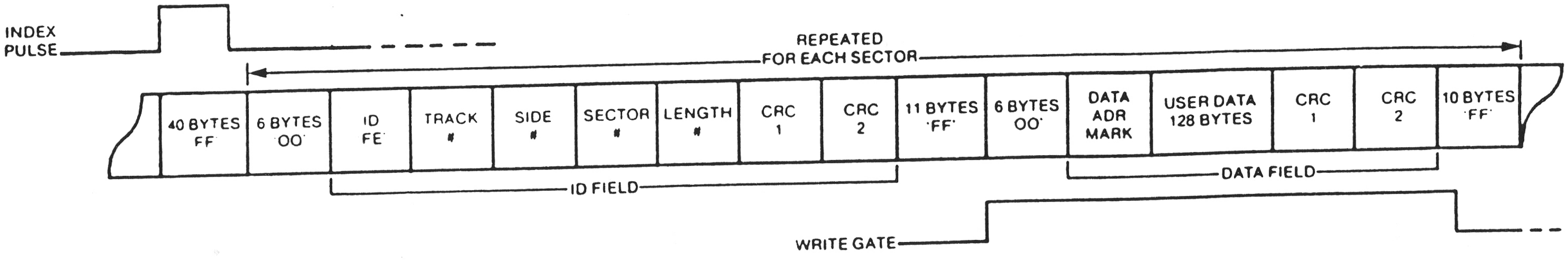
NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

*Write bracketed field 16 times.

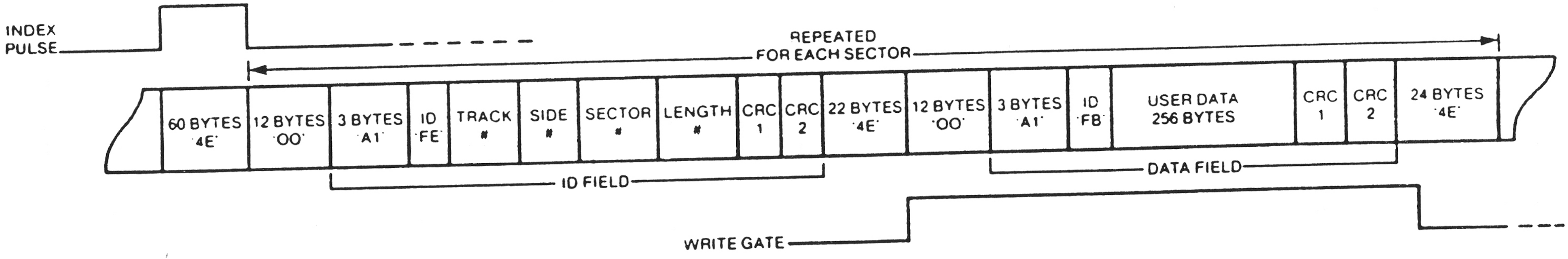
**Continue writing until WD1770 interrupts out. Approx. 369 bytes.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRC's written)
24	4E
668**	4E

*Write bracketed field 16 times.

**Continue writing until WD1770 interrupts out. Approx. 668 bytes.

1. Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.

2) Gap 2 cannot be varied from the recommended format.

3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD1770 Gap 1, 3, and 4 lengths can be as short as 2 bytes for WD1770 operation however PLL lock up time, motor speed variation write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00 3 bytes A1
Gap III**	10 bytes FF 4 bytes 00	24 bytes 4E 8 bytes 00 3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

STATUS REGISTER DESCRIPTION

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (6 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA/ TRACK 00	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when update. On Type I commands, this bit reflects the status of the TRACK 00 Pin.
S1 DATA REQUEST/ INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type I commands, this bit indicates the status of the Index Pin.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature .... −55°C to +125°C

Operating Temperature ...... 0°C to 70°C Ambient

Maximum Voltage to Any Input with Respect to V_{SS} .... (−15 to −0.3

DC OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
$_{IL}$	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_0 = -100\,\mu A$
V_{OL}	Output Low Voltage		0.40	V	$I_0 = 1.6\,mA$
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current	75 (Typ)	150	mA	

AC TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING — $\overline{RE}$ such that : R/$\overline{W}$ = 1, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TRE	RE Pulse Width of $\overline{CS}$	150			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		25	100	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			8000	nsec	
TDV	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 50 pf

No DRQ and INTRQ reset are fror . rising edge (lagging) of $\overline{RE}$, whereas resets are from falling edge (leading) of $\overline{WE}$.

WRITE ENABLE TIMING — $\overline{WE}$ suct. that : R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TAS	Setup ADDR to $\overline{CS}$	50			nsec	
TSET	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
TAH	Hold ADDR from $\overline{CS}$	20			nsec	
THLD	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
TWE	$\overline{WE}$ Pulse Width	150			nsec	
TDRW	DRQ Reset from $\overline{WE}$		100	200	nsec	
TIRW	INTRQ Reset from $\overline{WE}$			8000	nsec	
TDS	Data Setup to $\overline{WE}$	150			nsec	
TDH	Data Hold from $\overline{WE}$	0			nsec	

May 11, [illegible]

Jay Siegel

Brooklyn NY

Hi, Jay.

Here are the photocopies of the data sheet for the Western Digital 1770 chip.

If you refer to page 45 you will see under the column ARCHITECTURE the description of the track, sector, data, status, and command registers.

In the Zebra controller, these are accessed by the following port assignments:

Command/Status register	Port C0
Track register	C1
Sector register	C2
Data register	C3

The Data Request signal (DRQ) described on page 47 can be tested by bit 7 of port 2F.

One quick and easy way to see some of these in action is to use DDTZ.COM on the FORMAT.COM.

I hope your continuation of the FDD Express gets off to a good start. I'll be in contact with you soon by mail with a write up of some of the things I am working on.

I now have 3.5" DSDD drives running on my old model controller and I've been studying the 80 track format to see how it differs from the 40 track SSDD. I was able to find some of the formatting routine in the TOS code. My preliminary review shows that it first formats the first side of the disk with 80 tracks, 16 sectors per track, and 256 bytes per sector. This gives 80 tracks with 4K storage per track for a total capacity of 320K. It then selects side 2 of the disk and repeats the same operation to give another 320K storage capacity. The operating system is written to the first 4 tracks and the fifth track is reserved for the directory.

This means that of side 1, 20K is reserved for TOS and the directory leaving 300K for file storage on side 1. This plus the 320K on side 2 gives a total of 620K file storage capacity.

I'm testing some of the utilities I wrote which were published in Time Designs or which I uploaded to the Club Forum Library 14 of Compuserve and find that they do work on the 80 track disks. I need to investigate how TOS automatically switches from side 1 to side 2. My goal is to write a 80 track version of FORMAT.COM for the CP/M mode and to adjust those areas of CBIOS so the high density format can be used under CP/M.

I'll be in touch with you soon.

Best wishes,

Mike Finn

Michael C. Finn

Philadelphia PA